Docket No.: MIT9888

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Pitera et al.	**GROUP:**	**Unknown**
SERIAL NO:	Unknown	**EXAMINER:**	Unknown
FILED:	Herewith		

FOR: COPLANAR INTEGRATION OF LATTICE-MISMATCHED SEMICONDUCTOR WITH SILICON VIA WAFER BONDING VIRTUAL SUBSTRATES

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

INFORMATION DISCLOSURE STATEMENT

In compliance with 37 C.F.R. §§1.56, 1.97, and 1.98, Applicant submits copies of the documents listed on the attached Form PTO-1449.

The Commissioner is authorized to charge Deposit Order Account No. 19-0079 for any further fee that may be required.

Respectfully submitted,

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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below in an envelope, with sufficient postage as first class mail addressed to the Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria, VA 22313-1450, Attn: Mail Stop Patent Application

Deborah M. Costello

6/25/03
Date

FORM PTO-1449 (Rev. 5/92)	SAMUELS, GAUTHIER & STEVENS LLP 225 Franklin Street, Boston, MA 02110 Telephone: (617) 426-9180	ATTORNEY DOCKET NO. MIT9888 Pitera et al. APPLICANT: Herewith FILING DATE:	SERIAL NO. Unknown GROUP: Unknown EXAMINER: Unknown
INFORMATION DISCLOSURE STATEMENT BY APPLICANT			

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,882,987	3/16/99	Srikrishnan			8/26/97
	AB	5,374,564	12/20/94	Bruel			9/15/92
	AC	6,573,126	6/3/03	Cheng et al.			8/10/01
	AD	6,475,072	11/5/02	Cama[ero et al.			9/29/00
	AE	6,107,653	8/22/00	Fitzgerald			9/29/00
	AF	6,150,239	11/21/00	Goesele et al.			9/30/98
	AG	5,877,070	3/2/99	Goesele et al.			3/31/97

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES NO
	AH						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER INITIAL		
	AI	"Silicon on Insulator Material Technology"; M. Bruel; Electronics Letters; July 6, 1995; Vol. 31, No. 14; pgs: 12011202
	AJ	"Ge layer transfer to Si for photovoltaic applications"; Zahler et al., Thomas J. Watson Laboratory of Applied Physics, California Institute of Technology; pgs.: 558-562
	AK	"Transfer of 3 in GaAs film on silicon substrate by proton implantation process"; Jalaguier et al., Electronics Letters; February 19, 1998; Vol. 34, No. 4; pgs.: 408-409
	AL	"Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on Insulator (SGOI) Substrates"; Cheng et al., IEEE Electron Device Letters; Vol. 22, No. 7, July 2001; pgs.: 321-323
	AM	"Preparation of Novel SiGe-Free Strained Si on Insulator Substrates"; Langdo et al., IEEE International SOI Conference; 2002; pgs.: 211-212
	AN	"Cleaning and Polishing As Key Steps For Smart-Cut SOI Process"; Moriceau et al., IEEE International SOI Conference, October 1996; pgs: 152-153
	AO	"Relaxed Silicon-Germanium on Insulator Substrate By La;yer Transfer"; Cheng et al., Journal of Electronic Materials; Vol. 30, No. 12; 2001; pgs.: L37-L39

EXAMINER	DATE CONSIDERED

EXAMINER: **Initial if citation considered, whether or not citati n is in c nf rmance with MPEP 609; draw line through citation if n t in conformance and not c nsid red. Include c py f this form with n xt c mmunication t applicant.**